

REMARKS

Claims remaining in the present patent application are numbered 1-29. No amendments have been made. The rejections and comments of the Examiner set forth in the Office Action dated November 26, 2004 have been carefully considered by the Applicants. Applicants respectfully request the Examiner to consider and allow the remaining claims.

§112 Rejection

The present Office Action rejected Claims 1-29 under 35 U.S.C. §112, first paragraph, as containing subject matter which was not described in the specification in such a way as to reasonably convey to one skilled in the relevant art that the inventor(s), at the time the application was filed, had possession of the claimed invention. More particularly, the present Office Action objected to the claim limitation "a fixed pixel border having a predetermined width," as recited in Claims 1-3, 10, 13, 14, 19, and 20, and "a fixed dimension of n rows and m columns," recited in Claim 25.

For independent Claim 25, Applicant respectfully asserts that the pixel border region is not fixed. As such, the §112, first paragraph, is not proper and independent Claim 25 overcomes the §112 objection.

For independent Claims 1, 13, and 19, Applicants respectfully assert that there is sufficient support for a "fixed" pixel border, and a pixel border of "fixed" dimension. Applicants respectfully direct the Examiner to lines 15-21 on page 5 of the Summary. In particular, the specification describes a pixel border of width x . The width is not variable, but can be several pixels wide (e.g., $1 < x < 5$). That is, once width of x is determined, the pixel border is fixed. The specification provides a concrete example, as follows: "[in] one embodiment, the border region is two pixels wide" As such, the border region is fixed to two pixels.

Applicants respectfully disagree that the specification does not disclose the limitations of a "fixed" pixel border, and a pixel border of "fixed" dimension. That is, the specification contains support for the claimed limitation of a "fixed" pixel border, and a pixel border of "fixed dimension. In particular, Applicants respectfully point out that the specification recites that the "pixel border region 312 . . . [has] a predetermined pixel width, x ." (See lines 5-6, page 19). That is, the width of the pixel border region is predetermined to a width x . Applicants respectfully assert that because the pixel border region is predetermined, the

width x is not variable, but fixed. As such, the width x does not vary, but is a fixed variable.

In addition, the specification further supports a fixed pixel border region of width x . The specification states that the "width, x , of the pixel border region 312 is arbitrary" (See lines 11-12, page 19) That is, the pixel border region 312 is envisioned to be arbitrarily set to any number of fixed widths in various embodiments. In one case, x is equal to one pixel width. In another case, the width of the pixel border region, x , is equal to 5 pixels. In fact, as described previously, x can vary between 1 to 5 pixels, in various embodiments. In addition, the specification provides in the same sentence, that in one embodiment, the width of the pixel border region, x , is equal to 2 pixels. That is, x is fixed to 2 pixels.

Further, on page 21, lines 15-16, the specification recites that " $x=2$, but could be any width in accordance with the present invention." As stated previously, and as shown in Figure 9, the width of the pixel border is fixed to 2 pixels, in one embodiment. As stated, the pixel border could be increased or decreased in other embodiments, but the embodiment shown in Figure 9 shows a fixed pixel border region of 2 pixels.

Further, Figure 9 shows a pixel border region that is fixed to 2 pixels in width, where x is 2. As shown, the row drivers 450a-d and column drivers 440a-d are used for the pixel border region 312 and are uniformly driven by the threshold voltage drivers 430a and 430b. That is, no further control is shown for selecting between various rows and columns to vary the width of the pixel border region. As such, all the pixels in the pixel border region 312 are similarly driven and controlled. Thus, the pixel border region is fixed.

Also, on page 18, the frame buffer pixel region further supports a fixed border region that surrounds a frame buffer pixel region. The frame buffer pixel region contains a "matrix of discrete pixels . . . according to a variety of display dimensions and formats." That is, the frame buffer pixel region can be one of varying dimensions, in various embodiments. In one particular embodiment, the dimensions is fixed to 160 pixels to 160 pixels.

Thus, Applicants respectfully submit that the specification sufficiently supports a "fixed" pixel border, and a pixel border of "fixed" dimension. As such, Claims 1-29 overcome the 112 objections. Applicants respectfully request further examination of Claims 1-29.

35 U.S.C. §103 Rejection

The present Office Action rejected Claims 1-5, 8, 13-16, 19-23, 25, 26, 28, and 29 under 35 U.S.C. 103(a) as being unpatentable over the Taniguchi reference (U.S. Patent No. 4,824,212) in view of Yokota et al. (U.S. Patent No. 6,181,313). Applicants have reviewed the above cited references and respectfully submit that the present invention as described in embodiments of independent Claims 1, 13, 19, and 25, is neither anticipated nor rendered obvious by the Taniguchi reference taken alone or in combination with the Yokota et al. reference.

Independent Claims 1, 13, 19, and 25

Applicants respectfully point out that the present invention as described in embodiments of independent Claims 1, 13, and 19 includes, in part:

a fixed pixel border having a predetermined width, said fixed pixel border surrounding said passive matrix and comprising a plurality of pixels which are uniformly controlled between an on and off state by a common threshold signal.
(Emphasis Added)

Moreover, Applicants respectfully point out that the present invention as described in embodiments of independent Claim 25 includes, in part:

a pixel border surrounding said passive matrix and comprising a plurality of pixels which are uniformly controlled between an on and an off state by a common threshold signal.
(Emphasis Added)

Embodiments of the present invention as recited in independent Claims 1, 13, 19, and 25 pertain to a controllable pixel border for a negative mode passive matrix display device. In particular, the present invention as described in embodiments of independent Claims 1, 13, 19, and 25 recites that a pixel border, or fixed pixel border, that surrounds the passive matrix is uniformly controlled by a common threshold signal.

Applicants respectfully agree that the Taniguchi reference does not teach the limitations of a plurality of pixels which are uniformly controlled between an on and an off state by a common threshold signal, as is recited in independent Claims 1, 13, 19, and 25 of the present invention.

Moreover, Applicants respectfully note that the prior art reference, Yokota et al. fails to overcome the shortcomings of the Taniguchi reference. That is, the Yokota et al. reference also fails to teach or suggest the present display unit that comprises, in particular, the pixel border that surrounds a passive matrix, and is uniformly controlled between an on and off state by a common threshold signal, as claimed in independent Claims 1, 13, 19, and 25 of the present invention.

In contrast to independent Claims 1, 13, 19, and 25 of the present invention, the Yokota et al. reference, discloses a liquid display controller that can select part of the rows of a liquid crystal panel for display, such that the display is selectively produced on a portion of the liquid crystal display panel at a low voltage with a low-duty drive. In particular, the Yokota et al. reference, discloses a display unit comprising a liquid crystal panel that is capable of producing a display of up to four rows (see Figure 9 of the Yokota et al. reference).

The Yokota et al. reference is able to select rows in a liquid crystal panel for displaying an image, such that, the common drive signal is not applied to the rows in which the display is not produced. That is, non-display rows are in a stand-by state. That is, all of the rows in the Yokota et al. reference are capable of generating an image for display, and none are specifically assigned to be a pixels border.

Also, any of the rows are selectable to not produce an image for display. As such, the Yokota reference does not disclose a pixel border, but a display region that can partially select rows in the display to not display images. In addition, the Yokota et al. reference does not disclose a pixel border that surrounds a passive matrix for display,

since any two rows of the display can at best border two horizontal sides of one or more rows of the display.

In addition, Applicants respectfully disagree that with regards to Figures 14K and 14L the Yokota et al. reference teaches a pixel border that is uniformly controlled by a common threshold signal. In particular, for references purposes, the relevant section of the Yokota et al. reference is repeated below, as follows:

In the first frame (frame I), the selection level of the common signal OCM 2 is V1 and the non-selection level is V5. In the first frame (frame 1), the selection level of the segment signal SEG2 is GND and the non-selection level is V4. Any dot turns on when the voltage obtained by subtracting the potential of the segment signal from the potential of the common signal, exceeds the threshold value of the liquid crystal. The difference in the potential is used as a pixel signal D. therefore, the dot at the intersecting point of the transparent electrode ECOM2 and the transparent electrode ESEG2 is turned on. (See col. 14, lines 43-53)

In particular, Applicants respectfully assert that the Yokota et al. reference teaches that a dot, or pixel, is turned on when the voltage obtained by subtracting a segment signal from the common signal exceeds a threshold level of the liquid crystal. That is, generally any dot in the display matrix will turn on when the voltage applied to that dot exceeds a threshold level.

However, the Yokota et al. reference does not teach or disclose that dots corresponding to a pixel border are grouped together and uniformly controlled by a common control signal. Instead, the Yokota et al. reference teaches that those dots in the pixel border are each separately controlled and are turned on when the difference voltage of the segment and common signals exceeds the threshold value.

More particularly, Figure 14L in the Yokota et al. reference illustrates that each of the dots are separately controlled. For example, a dot (pixel) at the intersection of the signal electrodes COM2 and ESEG2, and another dot at the intersection of the signal electrodes COM 1 and ESEG1, are turned on. The rest of the dots as shown in Figure 14L are turned off. Conversely, the dot at the intersection of the signal electrodes COM 1 and ESEG2 is turned off. As such, the Yokota et al. reference shows that each dot is controlled separately, and that the dots are not uniformly controlled by a common control signal, which is in direct contrast to the claimed embodiments of the present invention, as recited in Claims 1, 13, 19, and 25.

The present invention, on the other hand, claims a display unit that has distinct display and border regions. In particular, the present invention also discloses a separate pixel border that surrounds the passive matrix

that is uniformly controlled between an on and off state by a common threshold signal, as recited in independent Claims 1, 13, 19, and 25 of the present invention.

Specifically, Figure 9 of the present Application describes the application of the common threshold signal to control the pixels in the fixed pixel border. The common threshold voltage is defined as the voltage difference between threshold voltage drivers 430a and 430b in their on or off states. In particular, the threshold voltage (V2) is applied to all the pixels of the fixed pixel border in the on state, and the threshold voltage (V1) is applied to all the pixels of the fixed pixel border in the off state.

Thus, Applicants respectfully submit that the present invention as disclosed in independent Claims 1, 13, 19, and 25 is not anticipated or rendered obvious by the Taniguchi taken alone or in combination with the Yokota et al. reference, and is in a condition for allowance. In addition, Applicants respectfully submit that Claims 2-12 which depend from independent Claim 1 are also in a condition for allowance as being dependent on an allowable base claim. Also, Applicants respectfully submit that Claims 14-18 which depend from independent Claim 13 are also in a condition for allowance as being dependent on an allowable base claim. Further, Applicants respectfully submit that Claims 20-24 which depend from independent

Claim 19 are also in a condition for allowance as being dependent on an allowable base claim. Additionally, Applicants respectfully submit that Claims 26-29 which depend from independent Claim 25 are also in a condition for allowance as being dependent on an allowable base claim.

CONCLUSION

In light of the facts and arguments presented herein, Applicants respectfully request reconsideration of the rejected Claims.

Based on the arguments presented above, Applicants respectfully assert that Claims 1-29 overcome the rejections of record. Therefore, Applicants respectfully solicit allowance of these Claims.

The Examiner is invited to contact Applicants' undersigned representative if the Examiner believes such action would expedite resolution of the present Application.

Respectfully submitted,

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